wiring patterns formed on the substrate in the circuit area;

a first dummy pattern which is formed of the same material as the wiring pattern, formed in the peripheral area, the dummy pattern encompassing the circuit area;

a first insulating layer formed on the circuit area and the peripheral area of the semiconductor substrate;

a second insulating layer formed on the first insulating layer which is formed on the semiconductor substrate, wherein the second insulating layer is not formed over the first dummy pattern; and

a third insulating layer formed on the exposed first insulating layer and the second insulating layer.

3 (amended). A semiconductor device as claimed in claim 2, wherein the first dummy pattern has a width, which is fixed by a concentration of solid content of the SOG layer.

4 (amended). A semiconductor device as claimed in claim 1, wherein the first dummy pattern has a width, which is designed for less than 1 μm where a concentration of solid content of the SOG layer is around 5.2 wt%.

5 (amended). A semiconductor device as claimed in claim 1, further

comprising;

a second dummy pattern formed under the first dummy pattern; and

a fourth insulating layer formed directly on the substrate and on the second dummy pattern, the fourth insulating layer including a thermally planarized surface,

whereby, the first dummy pattern is formed on the fourth insulating layer which is formed on the second dummy pattern, and the wiring patterns are formed on the fourth insulating layer.

10 (amended). A semiconductor device as claimed in claim 6, wherein each of the first and second dummy patterns has a width, which is designed for less than 1 μm where a concentration of solid content of the SOG layer is around 5.2 wt%.

11 (amended). A semiconductor device as claimed in claim 1, further comprising:

a third dummy pattern formed in the peripheral area between the first dummy pattern and the wiring patterns, the first insulating layer being not formed on the third dummy pattern.

13 (amended). A semiconductor device as claimed in claim 11, wherein the distance between the first dummy pattern and the third dummy pattern is designed

for over 0.9 μm.

14 (amended). A semiconductor device as claimed in claim 12, wherein each of the first and third dummy layer has a width, which is fixed by a concentration of solid content of the SOG layer.

15 (amended). A semiconductor device as claimed in claim 12, wherein each of the first and third dummy layer has a width, which is designed for less than 1 μm where a concentration of solid content of the SOG layer is around 5.2 wt%.

16 (amended). A semiconductor device as claimed in claim 1, further comprising:

a bonding pad formed on the semiconductor substrate in the circuit area; and

a fourth dummy pattern surrounding the bonding pad, the second insulating layer being not formed on the fourth dummy layer.

19 (amended). A semiconductor device as claimed in claim 17, wherein each of the first and fourth dummy layer has a width, which is fixed by a concentration of solid content of the SOG layer

20 (amended). A semiconductor device as claimed in claim 17, wherein each of the first and fourth dummy layer has a width, which is designed for less than

1 μm where a concentration of solid content of the SOG layer is around 5.2 wt%.

-- 27 (new). A semiconductor device, comprising:

a semiconductor substrate having a circuit area where an integrated circuit is formed and a peripheral area surrounding the circuit area;

wiring patterns formed on the substrate in the circuit area;

a dummy pattern which is formed of the same material as the wiring pattern, formed in the peripheral area, the dummy pattern encompassing the circuit area; and

an insulating layer formed above the semiconductor substrate, the insulating layer being formed outside the dummy pattern but not being formed over the dummy pattern, and the insulating layer having a moisture absorbable characteristic.

28 (new). A semiconductor device as claimed in claim 27, wherein the insulating layer is a second insulating layer, the semiconductor device further comprising first and third insulating layers formed on the substrate, the second insulating layer being located between the first insulating layer and the third insulating layer.

29 (new). A semiconductor device, comprising:

a semiconductor substrate having a circuit area where an integrated circuit is

formed and a peripheral area surrounding the circuit area;

wiring patterns formed on the substrate in the circuit area, the wiring pattern including a pad pattern;

a dummy pattern which is formed of the same material as the wiring pattern, formed in the peripheral area, the dummy pattern encompassing the circuit area; and

an insulating layer formed above the semiconductor substrate, the insulating layer being formed outside the dummy pattern but not being formed over the dummy pattern,

wherein the edge of the insulating layer is located on the pad pattern which is adjacent to the dummy pattern.

30 (new). A semiconductor device as claimed in claim 1, wherein the second insulating layer has a moisture absorbable characteristic.

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31 (new). A semiconductor device as claimed in claim 1, wherein the wiring patterns include a pad pattern, the edge of the second insulating layer being located on the pad pattern which is adjacent to the dummy pattern.

32 (new). A semiconductor device as claimed in claim 30, wherein the wiring patterns include a pad pattern, the edge of the second insulating layer being located on the pad pattern which is adjacent to the dummy pattern.